

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	3	du near chien-chih.in.	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 16:15
2	BRS	L2	0	pittkoun near saysamone.in.	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 16:16
3	BRS	L3	1927	438/257.ccls.	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:04

	Type	L #	Hits	Search Text	DBs	Time Stamp
4	BRS	L4	164	3 and (sacrificial)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:07
5	BRS	L6	292	(sacrificial near layer) near25 (mask or har-dmask) near25 (substrate)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:08
6	BRS	L5	295	(sacrificial near layer) near25 (mask or hardmask) near25 (substrate)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L7	295	(sacrificial near layer) near25 (mask or hardmask or hard-mask or hard near mask) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:29
8	BRS	L8	6149	(sacrificial near layer or silicon near nitride or sin) near25 (mask or hardmask or hard-mask or hard near mask) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:47
9	BRS	L9	1374	(sacrificial near layer or silicon near nitride or sin) near25 (mask or hardmask or hard-mask or hard near mask) near25 (substrate) near25 (remov\$3)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:31

	Type	L #	Hits	Search Text	DBs	Time Stamp
10	BRS	L10	334	(sacrificial near layer or silicon near nitride or sin) near25 (pattern\$3) near3 (mask or hardmask or hard-mask or hard near mask) near25 (substrate) near25 (remov\$3)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:38
11	BRS	L11	4146	(pattern\$3) near3 (mask or hardmask or hard-mask or hard near mask) near25 (substrate) near25 (remov\$3)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:38
12	BRS	L12	507	(pattern\$3) near3 (mask or hardmask or hard-mask or hard near mask) near25 (substrate) near25 (remov\$3) near25 (isolation or trench or sti)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:39

	Type	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L13	292	(sacrificial near layer) near25 (mask) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:52
14	BRS	L14	135	(pattern\$3 or etch\$3) near5 (sacrificial near layer) near25 (mask) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:58
15	BRS	L15	2358	(pattern\$3 or etch\$3) near5 (silicon near nitride or sin) near25 (mask) near25 (substrate)	US-PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/03 17:54

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	2186	(pattern\$3 or etch\$3) near5 (silicon near nitride) near25 (mask) near25 (substrate)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:54
17	BRS	L17	0	(pattern\$3 or etch\$3) near5 (silicon near nitride) near25 (mask) near25 (substrate) near25 (tunnel near dielectric)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:55
18	BRS	L18	11	(pattern\$3 or etch\$3) near5 (silicon near nitride) near25 (mask) near25 (substrate) near25 (tunnel\$3)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:56

	Type	L #	Hits	Search Text	DBs	Time Stamp
19	BRS	L19	3	(pattern\$3 or etch\$3) near5 (sin) near25 (mask) near25 (substrate) near25 (tunnel\$3)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:57
20	BRS	L20	5	(pattern\$3 or etch\$3) near5 (sacrificial) near25 (mask) near25 (substrate) near25 (tunnel\$3)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:57
21	BRS	L21	1710	(pattern\$3 or etch\$3) near5 (sacrificial near layer) near25 (substrate)	US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB	2005/01/0 3 17:58

	U	1	Document ID	Title	Current OR
1			US 20040070021 A1	Flash memory array with increased coupling between floating and control gates	257/314
2			US 20040029389 A1	Method of forming shallow trench isolation structure with self-aligned floating gate	438/694
3			US 20030011025 A1	Nonvolatile semiconductor memory device and manufacturing method thereof	257/316
4			US 20020195645 A1	Semiconductor device and method of manufacturing the same	257/314
5			US 6706601 B1	Method of forming tiny silicon nitride spacer for flash EPROM by using dry+wet etching technology	438/266
6			US 6649965 B2	Semiconductor device and method of manufacturing the same	257/314
7			US 6057580 A	Semiconductor memory device having shallow trench isolation structure	257/396

	U	1	Document ID	Title	Current OR
8			US 6034393 A	Nonvolatile semiconductor memory device using trench isolation and manufacturing method thereof	257/315
9			US 6027972 A	Method for producing very small structural widths on a semiconductor substrate	438/257
10			TW 550738 A	Method of forming shallow trench isolation structure with self-aligned floating gate	
11			TW 466756 A	PASTT memory cell of NAND type flash memory with small feature size and high program speed	

	U	1	Document ID	Title	Current OR
1			US 20040157434 A1	Method of manufacturing SONOS flash memory device	438/666
2			US 20040157422 A1	Methods for fabricating nonvolatile memory devices	438/594
3			US 20040152264 A1	Methods of manufacturing and-type flash memory devices	438/257
4			US 20040077107 A1	Method of making nanoscopic tunnel	438/1
5			US 20040129361 A	Defining an isolated magnetic region in film stack for fabricating magneto-resistive random access memory device, by forming mask defining protected and unprotected regions, and performing high-temperature etch of unprotected regions	